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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/027,359	CHONG, FAY
	Examiner	Art Unit
	Sheng-Jen Tsai	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/12/2002*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are presented for examination in this application (10,027,359).

Acknowledge is made of information disclosure document filed August 12, 2002.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 of copending Application No. **10/027,353**, as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other as explained in the "explanation" column of the table below:

10/027,359	10/027,353	EXPLANATION
1	1	Both describe similar apparatus with similar features/functions.
2	2	Both recite the cache memory being a dual-ported memory.
3	3	Both recite that cache memory comprises at least two independently interfaced memory banks.
4	4	Both recite that the cache is configured to indicate whether a particular block stored in the cache is modified with respect to a copy in main memory.
5	5	Both recite that the cache is to load a copy of operand from memory if it is not present in the cache.
6	6	Both recite that if all the block storage locations in the cache are currently storing valid data, the cache is to select one of the block storage location for overwriting.
7	7	Both recite the use of the least recently used algorithm to overwrite.

8	8	Both recite writing data back to memory before loading the copy to the selected storage location in cache.
9	13	Both recite the functional unit is to perform parity calculation on the block operands.
10	14	Both recite the command is issued by a storage system controller.
11	15	Both recite the first block operand is a first one of the data blocks in the stripe of data.
12	16	Both recite the functional unit is to perform the operation on two block-operands.
13	17	Both recite the same sources of the first and the second operands.
14	18	Both recite the same sources of the first and the second operands.
15	19	Both recite the cache is to store a word of the block result during an access cycle in which the cache is also to provide a word of block operand to the functional unit.
16	20	Both describe similar method of performing a block accumulation operation.
17	19	Both recite the cache is to store a word of the block result during an access cycle in which the cache is also to provide a word of block operand to the functional unit.
18	21	Both recite the cache memory being a dual-ported memory.
19	22	Both recite that cache memory comprises at least two independently interfaced memory banks.
20	23	Both recite that if all the block storage locations in the cache are currently storing valid data, the cache is to select one of the block storage location for overwriting.
21	24	Both recite the use of the least recently used algorithm to overwrite.
22	25	Both recite writing data back to memory if the data is modified with respect to a copy stored in the memory.
23	28	Both recite the functional unit is to perform parity calculation on the block operands and generate block results.
24	29	Both recite the command is issued by a storage system controller.
25	30	Both recite the functional unit is to perform the operation on two block-operands.
26	31	Both recite the second operand is to be provided from a data bus.
27	33	Both describe similar apparatus performing similar functions.
28	34	Both describe similar data processing system performing similar operations.
29	35	Both recite the same sources of the first and the second operands.
30	36	Both recite the same sources of the first and the second operands.
31	19	Both recite the cache is to store a word of the block result during an access cycle in which the cache is also to provide a word of block operand to the functional unit.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claim Rejections - 35 USC § 112

5. Claims 1-26,and 28-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the term "**cache accumulator**" is recited in statement "a **cache accumulator** coupled to the memory and the function unit, ..." It is noticed that the specification portion of the application refers to two terms when explaining the detailed operations of the invention, one as the "**cache accumulator**" and the other as the "**cache accumulator memory**." Instances referring the term "**cache accumulator**"

include the following (the page and line numbers cited below are referring to the specification section of the application filed):

- a cache accumulator that includes an associativity list. (page 7, line 4) ,
- the cache accumulator is configured to provide a block operand to the functional unit ... (page 4, line 6),
- the cache accumulator may include a dual-ported memory ... (page 4, line 12),

While Instances referring the term "**cache accumulator memory**" include the following:

- cache accumulator memory (50) is coupled to functional unit (25) ... (page 20, line 28),
- Cache accumulator memory (50) is configured as a cache for memory (15) ... (page 21, line 1),
- The cache accumulator memory banks (27A) and (27B) may be configured to be accessed using addresses in memory (15) ... (page 22, line 24),

The specification states that "FIG. 5 shows one embodiment of a system for performing block operations that includes a **cache accumulator memory** (50) (page 20, line 27)." According to Figure 5, the cache accumulator memory consists of three multiplexers (items 31, 32 and 23), two memory banks (27A and 27B), and a command/control unit which provides signals to the multiplexers. Thus, the scope and content of "**cache accumulator memory**" is well-defined and understood according to Figure 5. On the other hand, it is not clear as to what constitutes the "**cache accumulator**," and what is the difference between the "**cache accumulator memory**" and the "**cache accumulator**." To confuse the matter even further, the specification also states that

"e.g., **cache accumulator** (50) in FIG. 5 or **cache accumulator** (50A) in FIG. 9 (page 5, line 17)." Therefore item (50) of Figure 5 is referred to as the "**cache accumulator memory**" and "**cache accumulator**" in different occasions, which seems to imply that the "**cache accumulator memory**" and the "**cache accumulator**" are the same; however the context of the specification seems to suggest the "**cache accumulator**" is an entity that includes the "**cache accumulator memory**" and a functional unit capable of performing certain operations. Therefore,

- The scope and definition of the term "**cache accumulator**" needs to be clarified, and the distinction between the "**cache accumulator memory**" and the "**cache accumulator**" needs to be resolved,
- It is suggested that the term "**cache accumulator memory**" be used in claims 1-36 to replace the term "**cache accumulator**," as a functional unit is recited as a separate element of the disclosed apparatus/method/system,
- In the subsequent claim analysis, the examiner will treat the claims based on the "**cache accumulator memory**" instead of the "**cache accumulator**."

Claims 2-15 are rejected by virtue of their dependency on claim 1.

Claim 16 is rejected based on the same reason as provided for claim 1.

Claims 17-26 are rejected by virtue of their dependency on claim 16.

Claim 28 is rejected based on the same reason as provided for claim 1.

Claims 29-31 are rejected by virtue of their dependency on claim 28.

6. ***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4-6, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (U.S. 4,888,679).

As to claim 1, Fossum et al. disclose **an apparatus comprising:**

A memory [figure1 shows a main memory unit (item 23)];

A functional unit [figure 1 shows a vector processor unit (item 22) and a scalar processor (item 21), both are functional units] **configured to perform a block operation on one or more block operands to generate a block result** [a cache bypass is provided to transmit data directly to the vector processor as the data from the main memory are being stored in the cache (column 3, lines 1-4); the vector processor prefetch requests include the virtual address of the blocks that will be accessed by the vector processor (column 3, lines 20-22); Figure 2 shows that how blocks of data are stored in the main memory; and figure 7 shows that the vector processing unit having ADD, MASK and MULTIPLY sub-units for operating on the blocks of data]; **and a cache accumulator memory coupled to the memory and the functional unit** [figure 1 shows that a cache memory (item 24) is coupled to the main memory (item 23) and the functional unit (item 22, the vector processor and item 21, the scalar processor)], **wherein the cache accumulator memory is configured to provide a block operand to the functional unit and to store the block result generated by the functional unit** [figure 2 shows that blocks of data are to be transferred from the main memory to the cache, and then to the function unit (vector processor and scalar processor (see figure 1); figure 7 shows that the block data generated by both the vector processor (item 116) and the scalar processor (item 108) are piped through the

register file & arithmetic logic unit (item 111) and the cache bypass mux unit (item 135) to return to the data storage (item 114) of the cache unit (item 106)], **wherein the cache accumulator memory is configured to provide the block operand to the functional unit in response to receiving an instruction that uses an address in the memory to identify the block operand** [in response to a prefetch request, the cache is checked to determine whether it includes the required block, and if the cache does not have the required block, a refill request is sent to the main memory (column 2, lines 53-57); the vector processor receives a vector load instruction which commands the vector processor to send vector element addresses to the cache memory, and in response to those element addresses, the cache transmits the desired vector elements to the vector processor (column 4, lines 57-62); the cache includes means for storing selected predefined blocks of data elements, means for receiving requests from the scalar processor to access a specified data element, means for checking whether the data element is in a block stored in the cache, and means operative when data for the block including the specified data element is not so stored for reading the specified block of data from the main memory and storing the block of data in the cache (column 4, lines 25-33); If a data element needed by the scalar processor is not found in the cache, then the data element is obtained from the main memory, but in the process an entire block, including additional data, is obtained from the main memory and written into the cache. Due to the principle of locality in time and memory space, the subsequent times that the scalar processor 21 desires a data element, chances are that this data element will be found in the block which includes the previously

addressed data element. Therefore, chances are that the cache will already include the data element desired by the scalar processor (column 4, lines 36-47)].

As to claim 4, Fossum et al. do not explicitly mention that **the cache accumulator is configured to indicate whether a particular block operand stored in the cache accumulator is modified with respect to a copy of that particular block operand in the memory**, since the disclosure focuses on the aspect of vector processing using a data cache. However, it is inherent for all cache memory systems that a mechanism is required to maintain data coherency between the main memory and the cache memory, and as such an indicator, commonly known as the "dirty bit," is required to indicate whether the data in the cache has been modified and hence is different from the corresponding copy in the main memory. Therefore, this claim is anticipated by the invention of Fossum et al.

As to claim 5, Fossum et al. disclose that the cache includes means for storing selected predefined blocks of data elements, means for receiving requests from the scalar processor to access a specified data element, means for checking whether the data element is in a block stored in the cache, and means operative when data for the block including the specified data element is not so stored for reading the specified block of data from the main memory and storing the block of data in the cache (column 4, lines 25-33); and that If a data element needed by the scalar processor is not found in the cache, then the data element is obtained from the main memory (column 4, lines 36-37).

As to claim 6, a replacement policy, which overwrites a location in the cache with new data to be copied into the cache when all locations in cache are currently storing valid data, is an inherent property of any cache system. Further, Fossum et al. disclose that the cache includes an input address register generally designated, a tag store generally designated, and a data store generally designated. The data store is organized for storing selected ones of the predefined blocks of the data elements. In order to indicate whether data for a specified block are stored in the data store, the tag store is organized for storing respective tags associated with the blocks (column 6, lines 30-38). Also, as specifically shown in figure 2, the tag comprises the upper portion of the block address. In response to a fill request, an addressed block in the main memory is transferred to one or more predefined slots in the data store. The slots associated with a given block are indexed by an index j. The index j and the tag for a particular block specifies the block address for that block. Therefore, when an address of a desired byte is received in the input register, the index portion j points to at least one corresponding slot in the tag store and the addressed tag is fed to the comparator for comparison with the tag specified by the byte address (column 6, lines 41-52).

As to claim 12, Fossum et al. disclose that **the functional unit** [the vector processing unit shown in figure 7, item 116] **is configured to perform the operation on two block operands** [figure 7 shows that the vector processing unit performs ADD and MULTIPLY operations. Both ADD and MULTIPLY operations require two operands].

8. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of McClure (U.S. 5,590,307).

As to claim 2, Fossum et al. do not mention that **the cache accumulator memory comprises a dual-ported memory**. However, McClure explicitly discloses the invention of a dual-port data cache memory having one port dedicated to serving a local processor and a second port dedicated to serving a system (abstract, figure 2). A dual-port cache memory allows data to be transferred between the cache and other entities of the system, such as the main memory, at a higher speed as compared to a one-port cache memory. Since data transfer to and from the cache is unavoidable when a miss occurs, a higher data transfer speed will reduce the memory latency and improve the throughput of the system. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by a dual-port cache memory and to use it as the cache unit in the apparatus disclosed by Fossum et al. to further improve its performance.

As to claim 15, Fossum et al. do not mention that **the cache accumulator memory is configured to provide a word of the block operand to the functional unit during an access cycle in which cache accumulator also stores a word of**

the block result generated by the functional unit. However, McClure discloses the invention of a dual-port data cache memory having one port dedicated to serving a local processor and a second port dedicated to serving a system (abstract; figure 2). A dual-port cache memory allows two pieces of data to be accessed, one at each port, at the cache by other entity of the system at the same time, hence enabling the cache to serve the functional block with two pieces of data simultaneously (figure 2). In other words, the two-ported cache will be able to store a word of the block result from the functional unit (a write operation into the cache), and during the same access cycle provides a word to the functional unit (a read operation from the cache). This type of concurrent operations increases the system throughput. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by a dual-port cache memory in supporting concurrent operations, and to use it as the cache unit in the apparatus disclosed by Fossum et al. to further improve its performance.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of Faraboschi et al. (U.S. 6,122,708).

As to claim 3, Fossum et al. do not mention that **the cache accumulator memory comprises at least two independently interfaced memory banks,** although Fossum et al. do disclose the use of a plurality of main memory banks (figure 2, item 23) and teach that block interleaving of the memory bank addresses is useful in practicing the disclosed invention since vectors are stored and referenced in a linear

fashion with respect to the physical addresses of the bytes in the main memory. When a vector extends across one or more block boundaries, it is desirable for multiple ones of the contiguous blocks to be simultaneously accessed in the main memory using multiple banks (column 6, lines 6-13). Further, Faraboschi et al. discloses a data cache system for use with streaming data in which the data cache consists of two independently interfaced memory banks (figure 3, items 130 and 132), that The data cache memory may include a single bank, or two or more banks in a set associative configuration, with each bank includes a data cache, a tag array, and addressing circuitry (column 3, lines 47-50). Two-bank organization of the cache system allows data to be transferred to and from the cache system simultaneously using the two banks, such as **providing the block operand from a first storage location in a first one of the independently interfaced memory banks and to store the block result in a second block storage location in a second one of the independently interfaced memory banks** (this is the case where a vector/block extends across one or more block boundaries explained earlier), hence avoiding the situation where a single-bank cache becomes the bottleneck of memory access and will reduce the overall memory access latency. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by a two-bank cache memory architecture and to adopt it for the cache unit in the apparatus disclosed by Fossum et al. to further improve its performance.

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of

Handy, "The cache memory book: the authoritative reference on cache design," Academic Press, 1993, page 57.

As to claim 7, Fossum et al. do not explicitly mention that **the cache accumulator is configured to use a least recently used algorithm to select the first set of block storage locations to overwrite**, since the disclosure focuses on the aspect of vector processing using a data cache. However, Handy teaches that a replacement algorithm is required in a cache system to select which entry in the cache is to be replaced when a new line is to be brought into the cache, and that the least recent used algorithm is one of the most commonly adopted scheme. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the need to have a replacement algorithm and the benefit offered by a least recently used algorithm and to adopt it for the cache unit in the apparatus disclosed by Fossum et al.

As to claim 8, Fossum et al. do not explicitly mention that **if data in the selected one of the block storage locations is modified with respect to a copy of that data in the memory, the cache accumulator is configured to write the data back to the memory before loading the copy of the block operand into the selected one of the block storage locations**, since the disclosure focuses on the aspect of vector processing using a data cache. However, Handy teaches that a write strategy is required in a cache system to deal with the situations where data is modified in either he cache or the main memory, which leads to data inconsistency between the main memory and cache. Particularly, Handy teaches that a technique, known as "write –

through," in which the main memory is always updated first during all write cycles, is commonly adopted in cache system design (pages 64-65). With such a write-through policy, data consistency between the main memory and the cache will be enforced. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the need to have a write policy and the benefit offered by the write-through algorithm, and to adopt it for the cache unit in the apparatus disclosed by Fossum et al.

12. Claims 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of "Microsoft Computer Dictionary," Microsoft Press, 2002, page 391: parity.

As to claim 9, Fossum et al. do not mention that **the functional unit is configured to perform a parity calculation on the block operand**. However, parity is a well-known technique in the art and is commonly used for error checking/correction of data transmitted between a source and a destination to ensure the data integrity. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by the parity scheme for data integrity and to adopt it for the functional unit in the apparatus disclosed by Fossum et al. so that applications with heavy data traffic (there is a lot of data traffic between the cache memory and the main memory as well as the functional unit) are processed with high data reliability.

As to claim 10, refer to the claim analysis provided in "As to claim 9." Further, figure 7 shows the instructions/commands are provided by an instruction process unit (item 107).

As to claim 11, Microsoft Computer Dictionary specifically points out that **the parity may be calculated from a plurality of blocks in a stripe of data** [if checked on a block-by-block basis, the method is called longitudinal redundancy checking, or LRC (page 391)]. Further, Fossum et al. show in figure 2 that **the data to be processed is organized as a plurality of blocks** (BLOCK 0, BLOCK 1, BLOCK 2, etc. as items 26, 27 and 28 in figure 2) **which are distributed among a number of memory banks in a stripe of data** (figure 2, item 23); and since the functional unit disclosed by Fossum et al. includes a vector processor, which lends itself to operate on blocks of data very efficiently. As far as the sequence of the blocks is concerned, the blocks of data are to be loaded from the main memory into the cache and then into the vector processor, therefore the order of the data based on which the parity is to be calculated is preserved as the order by which the blocks are delivered from the main memory originally, hence **the first block operand is a first one of the data blocks in the stripe of data**.

13. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of Morton (U.S. 6,088,783).

As to claim 13, Fossum et al. do not explicitly mention that **the first operand is stored in the cache accumulator memory and the second operand is provided on**

a data bus coupled to provide operands to the functional unit. However, Morton discloses a Digital Signal Processing unit having a data cache (figure 1, item 108) and a plurality of functional units (figure 1, item 110~113, Arithmetic Units) and is capable of supporting both scalar and vector operations (figure 9, items 107 and 110/111/112/113). In figure 6, Morton shows that the operands may come form the X-bar Switch (item 619), which is directly connected to the data cache (figure 1, the data cache is connected to X-bar Switch via links 64b, and then to one of the ALU via another link 64b). Thus one of the operand to the functional unit (ALU) may come from the cache memory. In figure 6, Morton also shows that the second operand may come from an "Immediate Data" bus (item 620). Functional units capable of receiving data from various different sources allows operations requiring different data sources to proceed without waiting for a particular data to arrive, hence improve the throughput of the data processing system. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by a functional unit with multiple data sources in improving the system throughput and to incorporate it into the apparatus disclosed by Fossum et al. to further enhance the performance.

As to claim 14, Fossum et al. do not explicitly mention that **the first operand is stored in the cache accumulator memory and the second operand is provided from the main memory**. However, Morton discloses a Digital Signal Processing unit having a data cache (figure 1, item 108), a main memory (figure 1, items 101 and 116), and a plurality of functional units (figure 1, item 110~113, Arithmetic Units) and is

capable of supporting both scalar and vector operations (figure 9, items 107 and 110/111/112/113). In figure 6, Morton shows that the operands may come form the X-bar Switch (item 619), which is directly connected to the data cache (figure 1, the data cache is connected to X-bar Switch via links 64b, and then to one of the ALU via another link 64b). Thus one of the operand to the functional unit (ALU) may come from the cache memory. In figure 6, Morton also shows that the second operand may come directly from the memory bus (items C, 2C and C/2), thus the second operand may come for the main memory. Functional units capable of receiving data from various different sources allows operations requiring different data sources to proceed without waiting for a particular data to arrive, hence improve the throughput of the data processing system. Therefore it would have been obvious for persons of ordinary skills in the art at the time of applicant's invention to recognize the benefits offered by a functional unit with multiple data sources in improving the system throughput and to incorporate it into the apparatus disclosed by Fossum et al. to further enhance the performance.

Claim Rejections - 35 USC § 102

14. Claims 16, 20, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (U.S. 4,888,679).

As to claim 16, Fossum et al. a method of performing a block accumulation operation using a cache accumulation memory that comprises a plurality of block storage locations [refer to claim analysis provided in "As to claim 1"].

As to claim 20, refer to claim analysis provided in "As to claim 6."

As to claim 25, refer to claim analysis provided in "As to claim 12."

Claim Rejections - 35 USC § 103

15. Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 16 above, and further in view of McClure (U.S. 5,590,307).

As to claim 17, Fossum et al. show that the data stored in the main memory is such that successive words (words 0-63 in item 26 of figure 2) constitute the first block of operand (BLOCK 0 of figure 2) located within one bank (item 26, figure 2), and that successive words (words 64-127 in item 27 of figure 2) constitute the second block of operand (BLOCK 1 of figure 2) located within another bank (item 27, figure 2), and so on. Hence, when a block of data is loaded from the main memory into the cache, and then from cache to the functional unit, **successive words of the first block operand are provided**. Similarly, **successive words of a block of data will be stored from the functional unit to the cache, and then into to main memory**. Furthermore, with the dual-port data cache memory disclosed by McClure, **a word of the first block operand is provided from the cache to the functional unit during an access cycle in which a word of the block result is stored in the cache,** as explained in the claim analysis provided in "As to claim 15."

16. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 20 above, and further in view of McClure (U.S. 5,590,307).

As to claim 18, refer to claim analysis provided in "As to claim 2."

17. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of Faraboschi et al. (U.S. 6,122,708).

As to claim 19, refer to claim analysis provided in "As to claim 3."

18. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of Handy, "The cache memory book: the authoritative reference on cache design," Academic Press, 1993, page 57.

As to claim 21, refer to claim analysis provided in "As to claim 7."

As to claim 22, refer to claim analysis provided in "As to claim 8."

19. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of "Microsoft Computer Dictionary," Microsoft Press, 2002, page 391: parity.

As to claim 23, refer to claim analysis provided in "As to claim 9."

As to claim 24, refer to claim analysis provided in "As to claim 10."

20. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 20 above, and further in view of Morton (U.S. 6,088,783).

As to claim 26, refer to claim analysis provided in "As to claim 13."

Claim Rejections - 35 USC § 102

21. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (U.S. 4,888,679).

As to claim 27, refer to claim analysis provided in "As to claim 1."

Claim Rejections - 35 USC § 102

22. Claim 28 is rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (U.S. 4,888,679).

As to claim 28, refer to claim analysis provided in "As to claim 1."

Claim Rejections - 35 USC § 103

23. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 34 above, in view of Morton (U.S. 6,088,783), and further in view of "Microsoft Computer Dictionary," Microsoft Press, 2002, page 391: parity.

As to claim 29, refer to claim analysis provided in "As to claim 13" and "As to claim 9."

As to claim 30, refer to claim analysis provided in "As to claim 13" and "As to claim 11."

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. 4,888,679) as applied to claim 1 above, and further in view of McClure (U.S. 5,590,307).

As to claim 31, refer to claim analysis provided in "As to claim 15."

Conclusion

24. Claims 1-31 are rejected as explained above.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 8, 2004

PIERRE BATAILLE
PRIMARY EXAMINER